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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,040	02/20/2004	Eric Neyret	4717-10100	1950

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EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

3c

Office Action Summary	Application No.	Applicant(s)	
	10/784,040	NEYRET ET AL.	
	Examiner	Art Unit	
	Lex Malsawma	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-20* is/are allowed.

6)☒ Claim(s) *1,2,6 and 10-14* is/are rejected.

7)☒ Claim(s) *3-5,7-9 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 10 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by **Beitman** (4,795,718).

Regarding claims 1 and 2:

Beitman discloses a preventive treatment method for a multilayer semiconductor wafer that includes a supporting substrate 15 (Fig. 12), at least one intermediate layer 25/30 and a surface layer 35 in which an intermediate layer has an exposed lateral edge and the wafer is to be subjected to a subsequent treatment, which method comprises treating the wafer to cause a portion of the surface layer 35 to encapsulate the exposed lateral edge of the intermediate layer 25/30 with a portion of the surface layer 35 (Fig. 13) to prevent attack on the peripheral edge during the subsequent treatment (e.g., subsequent treatment to form contacts 45(A), 45(B)), wherein the treating comprises annealing the wafer by heating to a temperature and for a time sufficient to cause the surface layer portion 35 to cover the exposed lateral edge of the intermediate layer 25/30 (Figs. 12-13 and Col. 5, lines 17-21). Therefore, these claims are anticipated.

Regarding claims 10 and 11:

Beitman discloses subjecting the wafer to the subsequent treatment without detrimentally affecting the edge of the intermediate layer (note Fig. 14), wherein the subsequent treatment is a chemical attack on the exposed gate oxide layer 20 (note Col. 5, lines 25-28). Therefore, these claims are anticipated.

3. Claims 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Pribat et al. (4,952,526; hereinafter "**Pribat**").

Regarding claims 13 and 14:

Pribat discloses (in Figs. 2, 4, 5 and 11) a multilayer semiconductor wafer that includes a supporting substrate 1, at least on intermediate layer (20, 21 or 23) having an exposed edge lateral edge (Fig. 4), and a monocrystalline surface layer (30-34 in Fig. 11), wherein the exposed lateral edge of the intermediate layer (20, 21 or 23) is encapsulated with a portion of the monocrystalline surface layer (33 and/or 34 in Fig. 11) to prevent attack on the peripheral edge during subsequent treatments, wherein the wafer has an SOI structure (note Col. 6, lines 67-68). Therefore, these claims are anticipated.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Beitman** (4,795,718) in view of Iwamatsu et al. (6,150,696; hereinafter, "**Iwamatsu**").

Regarding claims 6 and 12:

Beitman anticipates the method of claim 1 but **lacks** the wafer having a silicon-on-insulator (SOI) structure or subjecting the wafer to a stabox process prior to the encapsulating step. Iwamatsu **teaches** semiconductor devices that incorporate SOI substrates have significant advantages over bulk devices such as that disclosed by Beitman, wherein some of the advantages include decreased junction capacitance and improved device isolation breakdown (note Col. 1, lines 15-18). Iwamatsu discloses that incorporating an SOI substrate would include the following steps: oxidizing the surface of the wafer to create oxide layer(s) "21" and/or "23" (Figs. 8 and 10) on the surface of the wafer by annealing at a temperature of about 1100 °C (Col. 10, lines 46-48); and deoxidation of the oxide is carried out by a chemical attack using a wet

etching solution (Col. 11, line 15-20), i.e., Iwamatsu discloses that incorporating an SOI substrate would include subjecting the wafer to a "stabox" process (note page 2, lines 14-21, of the current specification for steps used in a "stabox" process) prior to forming a semiconductor device such as a transistor (i.e., note transistors "MT" in Fig. 39 are formed well after the "stabox" step). It would have been obvious to one of ordinary skill in the art to modify Beitman by incorporating an SOI substrate/structure as taught by Iwamatsu because an SOI substrate would provide significant advantages over Beitman's bulk device. Note that Beitman modified as taught by Iwamatsu would result in performing the "stabox" process prior to Beitman's encapsulating step, since the encapsulating step is performed when forming a transistor.

Allowable Subject Matter

7. Claims 3-5, 7-9 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 16-20 are allowed.

9. The following is a statement of reasons for the indication of allowable subject matter:

Claims 3-5 and 16-20 are allowable primarily because the references of record, singly or in combination, cannot anticipate or fairly suggest a rapid thermal annealing (RTA) process performed at the temperature and time specified in claims 3 and 16, wherein the RTA process is sufficient to "flow" the surface layer such that a portion of the surface layer encapsulates the exposed lateral edge of the intermediate layer.

Claims 7-9 are allowable primarily because claim 7 requires the surface layer to be transferred from a donor wafer, i.e., transferred from a donor wafer prior to being treated to encapsulate the exposed lateral edge of the intermediate layer.

Claim 15 is allowable primarily because the surface layer must be a monocrystalline layer, which can be treated to encapsulate the exposed lateral edge while remaining monocrystalline, i.e., "the exposed lateral edge of the intermediate layer is encapsulated by the monocrystalline material".

Remarks

10. Applicant's remarks/arguments have been carefully reviewed and considered; however, in reference to claims 1, 2, 6 and 10-14, they are moot in view of the new grounds of rejections, which are necessitated by the amendments made to claims 1 and 13.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lex Malsawma

March 29, 2005

OLIK CHAUDHURI
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